Amendments to the Claims

Claims 1-34 (Canceled).

35. (Currently Amended): A method ~~forming~~ of forming a local interconnect comprising:

forming at least two transistor gates over a semiconductor substrate;

depositing a local interconnect layer to overlie at least one of the transistor gates and interconnect at least one source/drain region proximate one of the transistor gates with semiconductor substrate material proximate another of the transistor gates;

implanting at least one dopant into the local interconnect layer in at least two implanting steps, one of the two implanting steps providing a peak implant location in a first portion of the layer which is deeper within the layer than a peak implant of the other implanting step; and

diffusing at least some of the dopant from the local interconnect layer into semiconductor substrate material therebeneath.

36. (Previously Presented): The method of claim 35 comprising conducting the one implanting step relative to another portion of the local interconnect layer to have a peak implant location extending through said layer and into the semiconductor substrate material therebeneath.

37. (Previously Presented): A method of forming a local interconnect comprising:

forming at least two transistor gates over a semiconductor substrate;

depositing a local interconnect layer to overlie at least one of the transistor gates and interconnect at least one source/drain region proximate one of the transistor gates with semiconductor substrate material proximate another of the transistor gates; and

implanting at least one dopant through the local interconnect layer into semiconductor substrate material therebeneath.

38. (Previously Presented): The method of claim 37 further comprising in another implanting step separate from said implanting, implanting at least one dopant to a peak concentration location which is entirely within the local interconnect layer.

Claims 39-63 (Canceled).

64. (Previously Presented): The method of claim 35 wherein the semiconductor substrate material comprises bulk substrate material.

65. (Previously Presented): The method of claim 35 wherein the semiconductor substrate material comprises bulk monocrystalline silicon.

66. (Previously Presented): The method of claim 35 wherein the two implanting steps implant dopants which are of the same conductivity type.

67. (Previously Presented): The method of claim 35 wherein the two implanting steps implant dopants which are of different conductivity type.

68. (Previously Presented): The method of claim 35 wherein the two transistor gates each comprise an insulative cap, and wherein the deeper one implanting step also provides a peak implant location which is received within the insulative cap of at least one of the transistor gates.

69. (Previously Presented): The method of claim 68 wherein the deeper one implanting step also provides a peak implant location which is received within the insulative cap of both of the transistor gates.

70. (Previously Presented): The method of claim 35 wherein the two transistor gates each comprise at least one anisotropically etched insulative sidewall spacer, and wherein the deeper one implanting step also provides a peak implant location which is received within at least one of the anisotropically etched insulative sidewall spacers.

71. (Previously Presented): The method of claim 70 wherein the deeper one implanting step also provides a peak implant location which is received within insulative sidewall spacers of both of the transistor gates.

72. (Previously Presented): The method of claim 70 wherein the two transistor gates each comprise an insulative cap, and wherein the deeper one implanting step also provides a peak implant location which is received within the insulative cap of at least one of the transistor gates.

73. (Previously Presented): The method of claim 72 wherein the deeper one implanting step also provides a peak implant location which is received within the insulative cap of both of the transistor gates.

74. (Previously Presented): The method of claim 37 wherein the semiconductor substrate material comprises bulk substrate material.

75. (Previously Presented): The method of claim 37 wherein the semiconductor substrate material comprises bulk monocrystalline silicon.

76. (Previously Presented): The method of claim 37 wherein the two transistor gates each comprise an insulative cap, and wherein the implanting also provides a peak implant location which is received within the insulative cap of at least one of the transistor gates.

77. (Previously Presented): The method of claim 76 wherein the implanting also provides a peak implant location which is received within the insulative cap of both of the transistor gates.

78. (Previously Presented): The method of claim 37 wherein the two transistor gates each comprise at least one anisotropically etched insulative sidewall spacer, and wherein the implanting also provides a peak implant location which is received within at least one of the anisotropically etched insulative sidewall spacers.

79. (Previously Presented): The method of claim 78 wherein the implanting also provides a peak implant location which is received within insulative sidewall spacers of both of the transistor gates.

80. (Previously Presented): The method of claim 78 wherein the two transistor gates each comprise an insulative cap, and wherein the implanting also provides a peak implant location which is received within the insulative cap of at least one of the transistor gates.

81. (Previously Presented): The method of claim 80 wherein the implanting also provides a peak implant location which is received within the insulative cap of both of the transistor gates.